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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/583,233 | 05/31/2000 | Tomomi Furudate | P108397-00011 | 3618 |

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| EXAMINER | |
|---|---|
| HO, THANG H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | 11 |

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/583,233 | Applicant(s) FURUDATE ET AL. | |
|---|---|---|---|
| | Examiner Thang H Ho | Art Unit 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3,5-7 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-7 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 360579, filed on 12/20/1999.

2. Claims 1, 3, 5-7, and 9-12 are pending in this application for examination.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, 5-7 and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Imura et al. (USPN 5,398,212).

As per **claims 1, 5 and 9**, Imura discloses in FIG. 5 the system and method for controlling a semiconductor device, comprising: a plurality of memory cells [**memory cell array 3**] corresponding to an address space larger than $2^n$ and smaller than $2^{(n+1)}$ [**address signal $A_0$-$A_n$**], where n is a positive integer; and an invalid address detecting circuit [**empty address detecting circuit 5**] for detecting that an address signal supplied from exterior indicates an address space other than the address space (e.g. column 5, lines 31 through column 6, lines 11); an invalid signal outputting circuit [**output buffer circuit**

4] for outputting an invalid signal [**e.g., outputting high impedance state thereby indicating that the address signal is invalid**] to the exterior [DATA $D_0$-$D_i$] of the semiconductor memory device when the invalid address detecting circuit carries out the detection [**Table 2 and column 8, lines 21-67**]; and an output controlling circuit [**control circuit 6**] for outputting, when the invalid address detecting circuit carries out the detection in a read operation, a data signal having been accessed and read in advance [**e.g., outputting high impedance state when the empty address detecting circuit detects an empty or invalid address (Table 2 and column 8, lines 21-67). Furthermore, the control circuit 6 may be programmed to access a non-empty address when the address signal specifies an empty address (Figure 2 and column 6, lines 52-54)**].

As per **claims 3 and 6**, Imura discloses that the device further comprising an output circuit [**output buffer circuit 4**] for receiving a read data signal from the memory cells and continuously outputting the data received in advance to the exterior, according to a control by the output controlling circuit when the invalid address detecting circuit carries out the detection in the read operation [**"Alternatively, the control circuit 6 may be programmed to access a non-empty address when the address signal specifies an empty address.", (see Figure 2 and column 6, lines 52-54)**].

As per **claims 7 and 10**, Imura discloses system and method further comprises a command controlling circuit for carry out a write or an erase operation in the memory

cells in response to a command input from the exterior, wherein the command controlling circuit invalidates the command input to thereby prohibit the write or the erase operation, when the invalid address detecting circuit detect that the address signal supplied from exterior as the command input indicates the address space other than the address space **["The present invention is applicable to various semiconductor memory devices, such as mask ROMs (Read-Only Memories), DRAMs (Dynamic Random Access Memories), SRAMs (Static RAMs), EPROM (Erasable Programmable ROMs), EEPROMs (Electrically EPROMs), and flash EEPROMs.", (column 5, lines 17-22)]**.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura et al. (USPN: 5,398,212), hereinafter Imura.

Imura discloses the semiconductor memory device substantially as claimed including: a decoder, which decodes the address signal **[see FIG. 5]** a sense amplifier **[see column 5, lines 57-58]** which amplifies a data signal read from the memory cells. Imura also teaches the method for deactivating (inactivating) the output buffer circuit (4) to reduce power consumption through the use of an internal control signal (/E) to control the output buffer via the output control circuit (7), when the address detecting circuit

carries out the detection [**FIG. 6, column 9, line 24 through column 10, line 30**]. However, Imura fails to specifically teach the deactivations of the decoder and the sense amplifier when the invalid address detecting circuit carries out the detection. Official Notice is taken that it would have been obvious for one skilled in the art at the time the invention was made to implement the semiconductor memory device as taught by Imura and to include the deactivations of the address decoder (2) and the sense amplifier, in addition to the deactivation of the output buffer circuit 4, to further reduce power consumptions in order to provide a low-cost semiconductor memory device as pointed out by Imura on column 10, lines 24-25.

***Conclusion***

7. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to (703) 872-9306

Hand–delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 3:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thang Ho
Art Unit 2188
May 27, 2004

Mano Padmanabhan
5/27/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER